Hall Ticket Number:

Code No. : 15433 S

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.C.E.) V-Semester Supplementary Examinations, June-2022

Computer Organization &Architecture

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10× 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Distinguish between Computer Architecture and Organization.	2	1	1	1
2.	Represent the number (-46.75) in IEEE 754 single and double precision representation.	2	1	1	2
3.	Draw the Block Diagram of Hardwired Control unit for basic computer. How many Decoders are required?	2	1	2	2
4.	Match the following: A) MOV A,D — 1. Direct Addressing Mode B) MVI B,23H — 2. InDirect Addressing Mode C) STA 2345H — 3. Register Addressing Mode D) MOV A,M — 4. Implied Addressing Mode E) CMA — 5. Immediate Addressing Mode	2	1	2	2
5.	Write the classification of Parallel Processors.	2	1	3	1
6.	What is a Vector Processor? List any Two applications of Vector Processors.	2	1	3	3
7.	Differentiate between Memory mapped I/O and Isolated I/O.	2	1	4	2
8.	List the functions of I/O Interface.	2	1	4	2
9.	Write the order of Memory Hierarchy in Computer Organization.	2	1	5	2
10.	How many 512 X 8 RAM Chips are needed to design a Memory Capacity of 8 K Bytes? What is the size of Address Bus?	2	2	5	3
	Part-B (5×8 = 40 Marks)				
11. a)	Draw the Flow chart for Signed Magnitude Multiplier and explain the multiplication process step by step for the operands (-5) and 9.	4	3	1	3
b)	Differentiate between Restoring and Non Restoring Division Algorithm with an example.	4	3	1	2
12. a)	Describe the address Sequencing capabilities of Micro Programmed Control unit.	4	2	2	2
b)	Explain the importance of ALE, INTR, HLDA and SID signals with necessary examples.	4	3	2	2

Contd... 2

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13. a)	Write the key differences between RISC and CISC Processors	4	2	3	2
b)	Consider a non pipelined Processor with a Clock rate of 2.4 GHz and average cycles per instruction of 4. The same Processor is upgraded to a pipeline Processor with 5 stages. But due to the Internal Register delay, the clock speed is reduced to 2GHz. Calculate the Speedup factor of the pipeline Processor to complete 100 Tasks.	4	4	3	3
14. a)	Discuss different types of Asynchronous Data Transfer methods.	4	2	4	2
b)	Explain about Daisy Chaining method of handling the interrupts with a neat diagram?	4	2	4	1
15. a)	Explain the working of Content Addressable Memory. Identify the importance of Augment Register and Key Register.	4	2	5	2
b)	A Computer is having 4GB of Main Memory and 2MB of Cache Memory and the Block Size is 512 Bytes. Find the number of bits needed to represent Tag, Set Index, Block Offset. ***Note: Cache uses Direct Mapping***	4	4	5	3
16. a)	Explain the hardware requirement for Signed magnitude addition /subtraction algorithm.	4	3	1	2
b)	Draw the Block Diagram of 8085 and explain the Register Organization	4	2	2	2
17.	Answer any ***two*** of the following:				
a)	Performance Issues in Pipeline Processors.	4	2	3	2
b)	DMA Controller Block Diagram and its working.	4	2	4	2
c)	What do you mean by Virtual Memory? Discuss how paging helps in implementing Virtual Memory.	4	2	5	2

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%

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ECE